

8-PSK CODED TDMA SATELLITE DEMODULATOR

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FINAL BRIEFING

**ADVANCED TECHNOLOGY SATELLITE DEMODULATOR
DEVELOPMENT**

NAS3-24678

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ABBREVIATIONS USED IN BRIEFING

• ACI	adjacent channel interference
• AMTD	Advanced Modulation Technology Development
• ASIC	application specific Integrated circuit
• AWGN	additive white Gaussian noise
• BER	bit error rate
• CCI	co-channel interference
• codec	coder/decoder
• ECL	emitter coupled logic
• MCD	multi-channel demultiplexer and demodulator
• MMIC	monolithic microwave integrated circuit
• modem	modulator/demodulator
• SAW	surface acoustic wave
• TDMA	time division multiple access

EXECUTIVE SUMMARY

- OBJECTIVES
- REQUIREMENTS
- PHASES
- COSTS AND DURATION
- PROOF-OF-CONCEPT MODEL BLOCK DIAGRAM
- PROOF-OF-CONCEPT MODEL PHYSICAL CONFIG.
- PERFORMANCE OF POC MODEL
- CONCLUSIONS OF PROGRAM
- RECOMMENDATIONS FOR FUTURE

OBJECTIVES:

- Develop a proof-of-concept uplink modulation system which will significantly increase the bandwidth efficiency of a TDMA uplink system
- Maintain present performance levels
- POC model should exhibit potential for low weight and power consumption

SALIENT REQUIREMENTS FROM RFP:

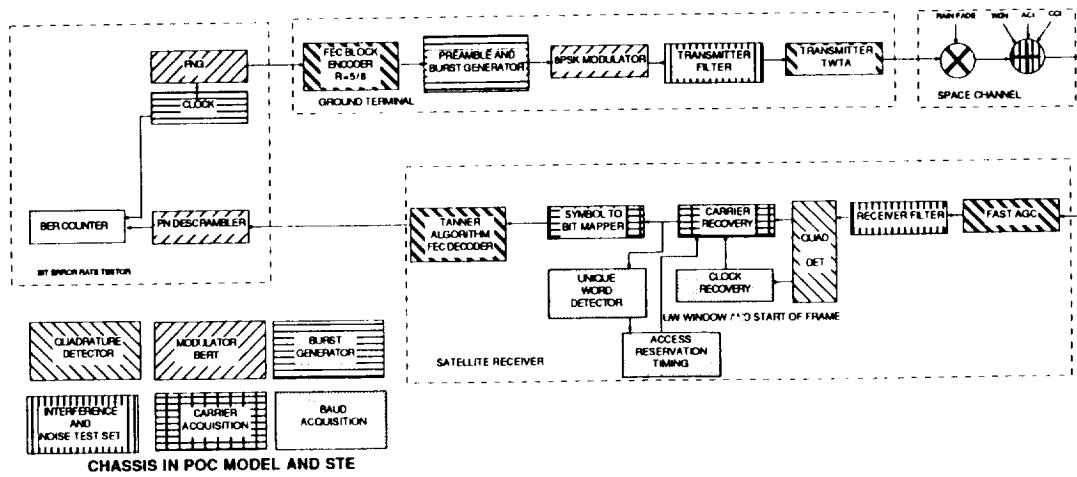
- Bandwidth Efficiency > 2 bits/ sec/ Hz
- Implementation loss < 2 dB
- 1 dB degradation in 20 db ACI or CCI
- TDMA burst mode with preamble < 100 bit periods
- Throughput > 200 Mbps

DERIVED REQUIREMENTS:

- 8PSK modulation
- Nyquist filter with rolloff factor of 0.2
- CCI spec requires forward error correction coding
- Mostly digital mechanization for eventual ASIC design

PHASES:

- Refine preliminary design
- Develop preliminary design
- Build and test breadboard
- Plan, specify, and fab POC model
- Test POC model and establish POC
- Product assurance



BLOCK DIAGRAM OF GROUND AND SATELLITE TDMA TEST SYSTEM

CONCLUSIONS OF PROGRAM

- CONCEPT OF THE POWER AND BANDWIDTH EFFICIENT SATELLITE DEMODULATOR HAS BEEN PROVEN WITHIN THE BUDGETARY CONSTRAINTS OF THE PROGRAM
- BANDWIDTH EFFICIENCY COULD BE DEMONSTRATED (I.E., ACI SPEC MET) THROUGH FILTER IMPROVEMENTS
- POWER EFFICIENCY COULD BE DEMONSTRATED (I.E., BER SPEC MET IN AWGN) THROUGH IMPROVEMENTS IN CLOCK RECOVERY LOOP AND FILTERS
- DIGITAL PORTION OF THE SATELLITE DEMODULATOR COULD BE REALIZED IN TWO GATE ARRAYS PLUS SOME MEMORY CHIPS, ANALOG PORTION COULD BE GREATLY REDUCED IN SIZE AND WEIGHT BY UTILIZING SAW FILTERS AND AN MMIC QUADRATURE DETECTOR
- CODEC PERFORMANCE WITH DEMOD IN CCI PROVEN BY SIMULATION

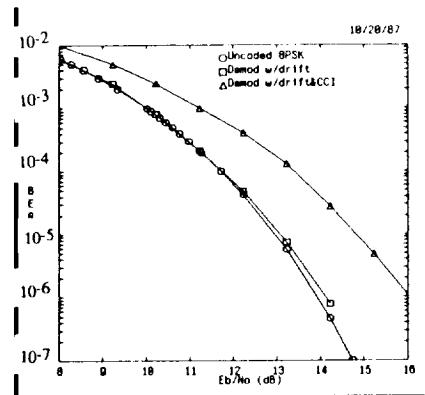
RECOMMENDATIONS FOR FUTURE

- CONTINUE SATELLITE MODEM DEVELOPMENT IN COMPACT FORM
 - (A) ASIC REALIZATION OF DIGITAL PORTION (TWO ECL GATE ARRAYS)
 - (B) DEVELOPMENT OF STEEP SKIRTED NYQUIST FILTERS IN SAW TECHNOLOGY AT ABOUT 300 MHz
 - (C) MMIC OR HYBRID QUADRATURE DETECTOR AND LO
- CONTINUE DEVELOPMENT OF SATELLITE CODEC IN ASIC
- CONTINUE DEVELOPMENT OF LOW BIT RATE MCD IN ASIC AND/OR DSP

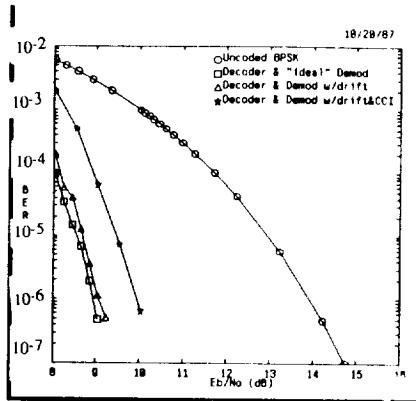
SPECIFICATIONS OF POC MODEL

PARAMETER	VALUE	TEST SPEC. NO. OR METHOD OF DETERMINING COMPLIANCE
Bandwidth	> 2 Bits/sec/Hz	1
Efficiency		
Bit Rate	240 Mbps	by design
Channel Spacing	96 MHz	by design
Transmission Mode	TDMA	by design
Frame Length	1 ms	by design
Preamble (CW portion) (UW portion)	32 symbols 8 symbols	by design
Receive Frequency	3.373056 GHz±1.5KHz	by design
Input level at receiver filter	-30 dBm±0.5 dB	by design
BER at Es/No=21 dB	< 5 x 10 ⁻⁷	2
Degradation Due to +20 dB ACI	< 1 dB	3
Degradation Due to -20 dB CCI	< 1 dB	3
Probability of bit error due to missing unique word	< 1 x 10 ⁻⁷ at Es/No =13 dB	by computation (4)
Probability of Carrier Cycle Slip	< TBD at Es/No= TBD dB	5
Bit-timing Jitter	< 125 ps RMS	6
Probability of Clock Cycle Slip	< TBD at Es/No=TBD dB	7
Minimum Guard Time Between Bursts	25 ns	by design of STE

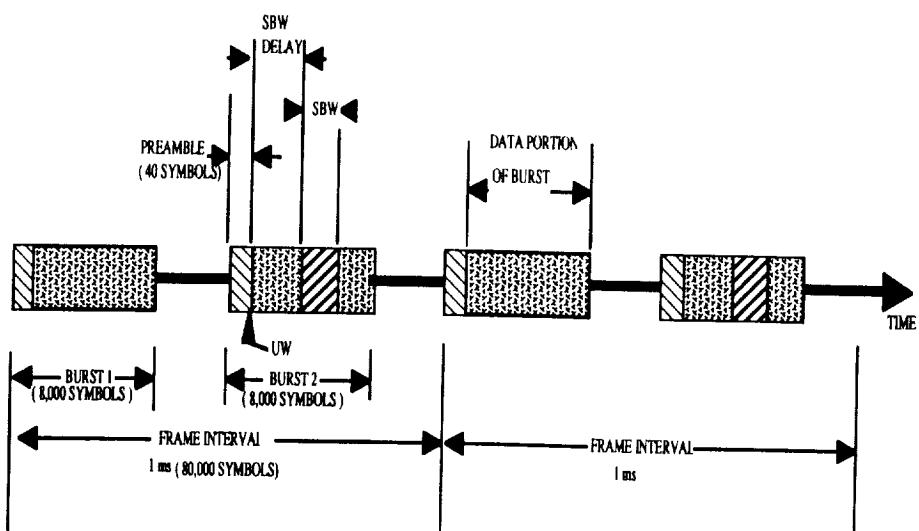
SIMULATIONS OF DEMOD PERFORMANCE WITH DRIFT AND CCI



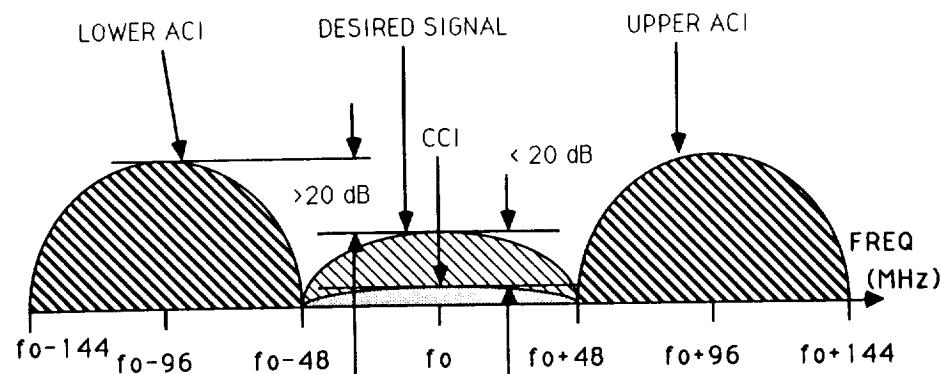
SIMULATIONS OF DEMOD AND DECODER PERFORMANCE WITH DRIFT AND CCI



PREAMBLE AND BURST STRUCTURE



SIGNAL SPECTRA SHOWING CO-CHANNEL AND ADJACENT-CHANNEL INTERFERENCES



AMTD INTERFERENCE AND NOISE TEST SET CHASSIS

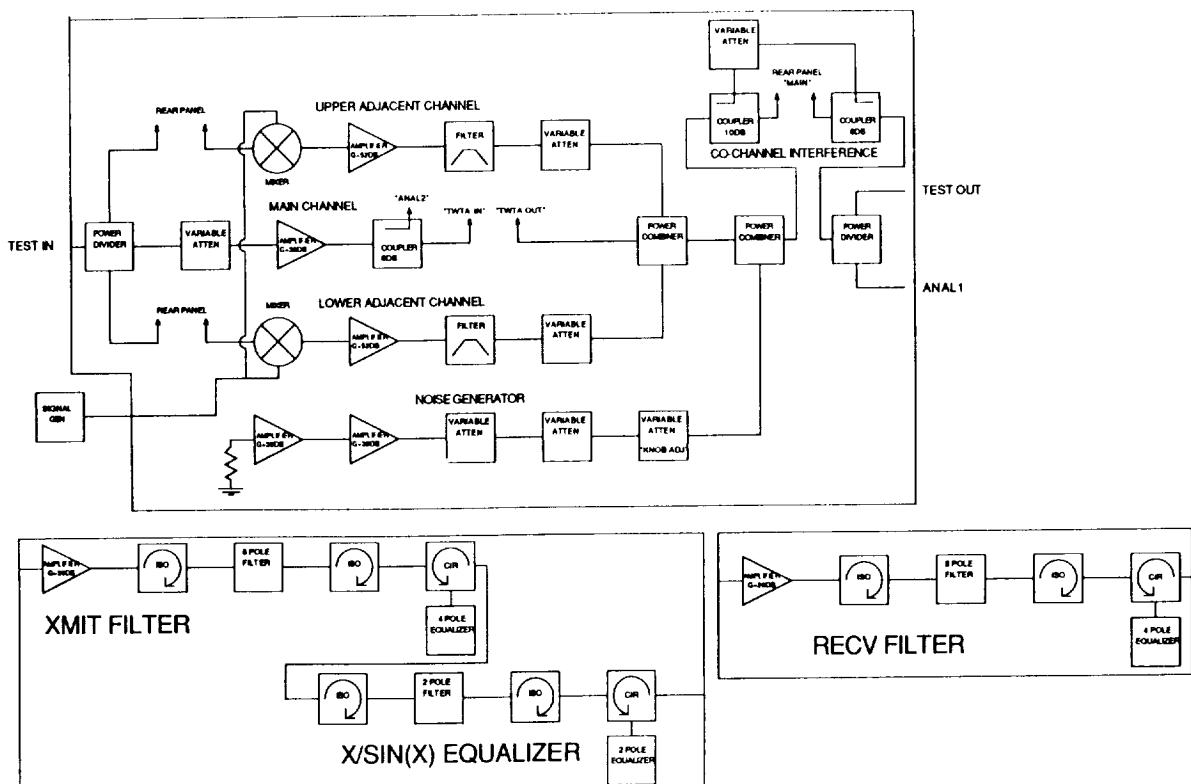
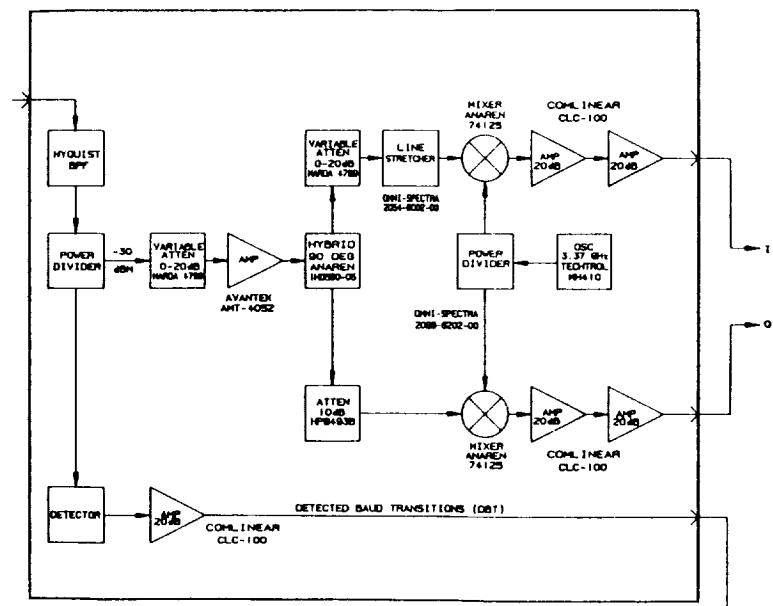
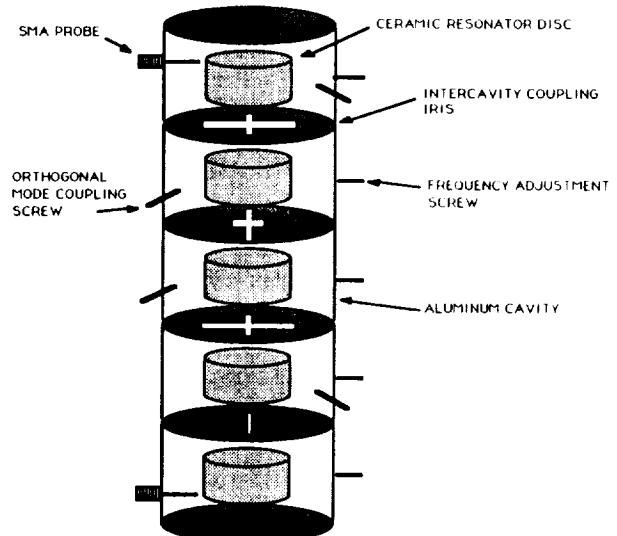
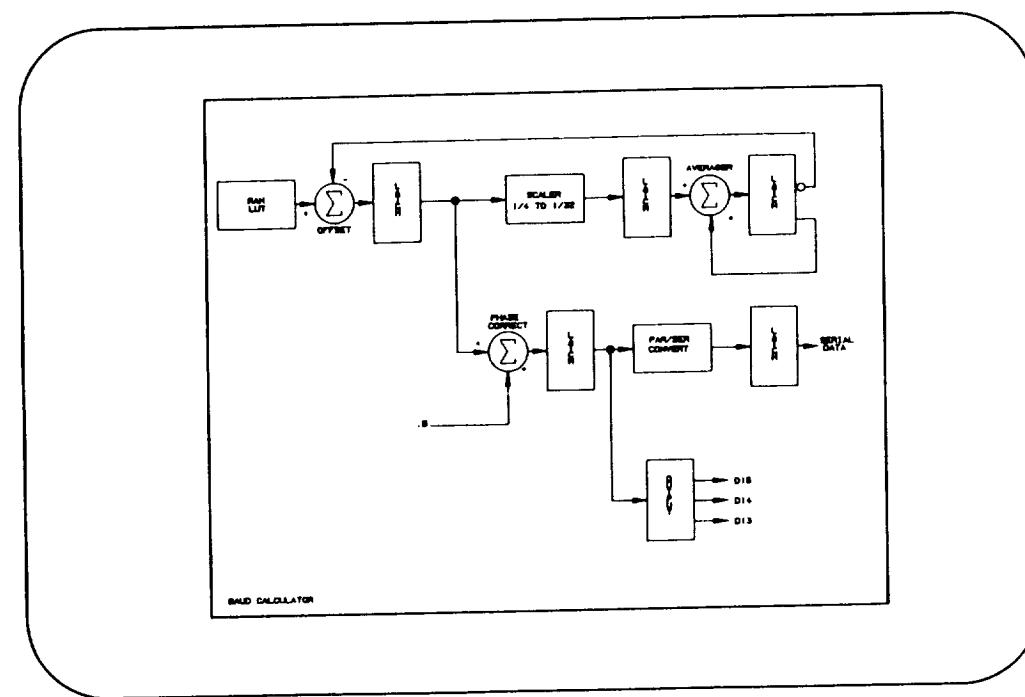
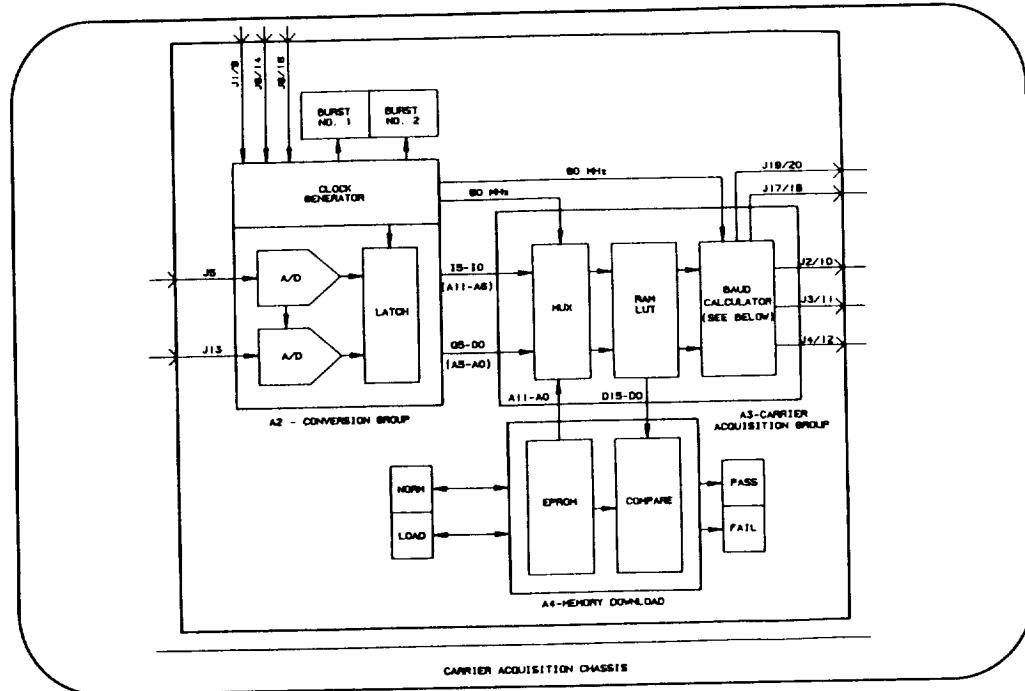


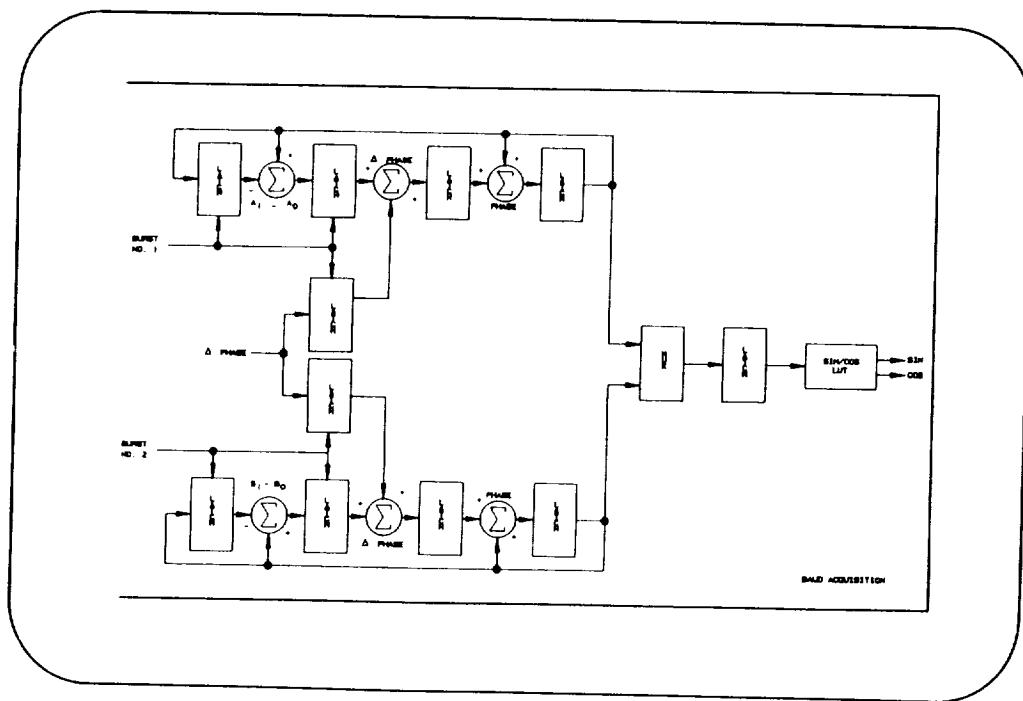
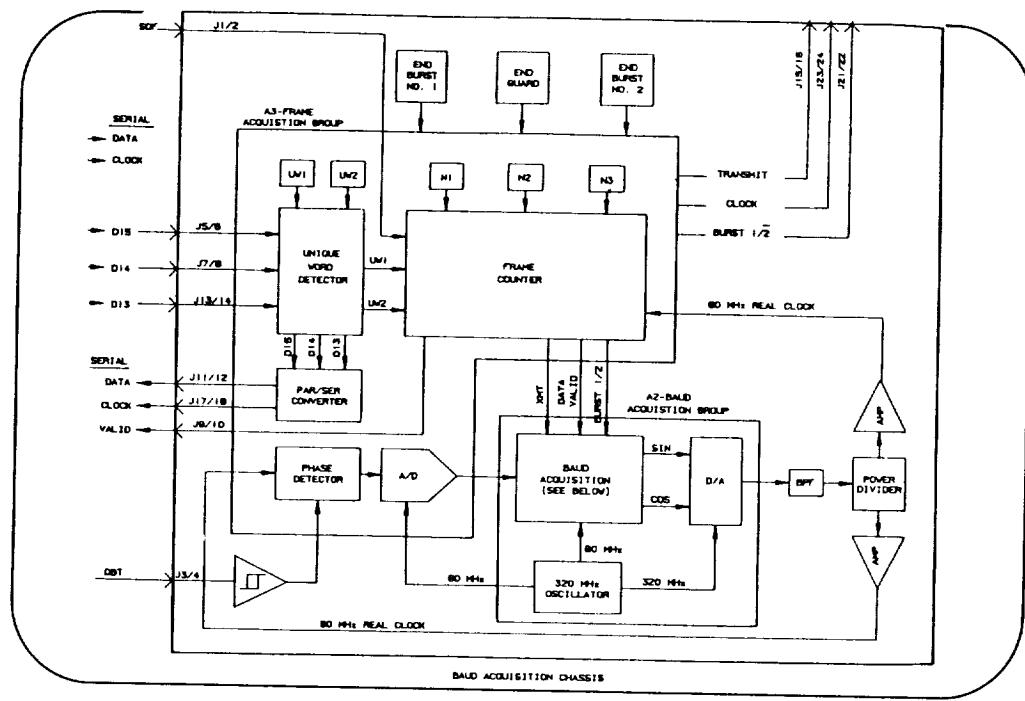
Figure 1 Interference/Noise Generator Block Diagram

MECHANICAL CONFIGURATION OF NYQUIST FILTERS

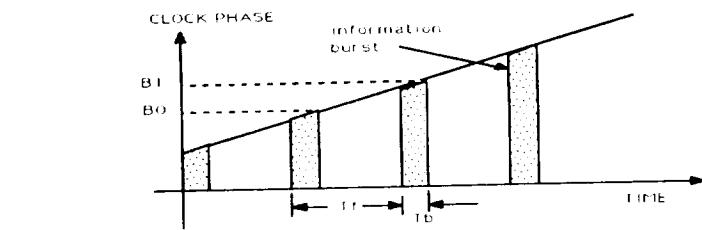
9 Pole Dielectric Resonator Filter





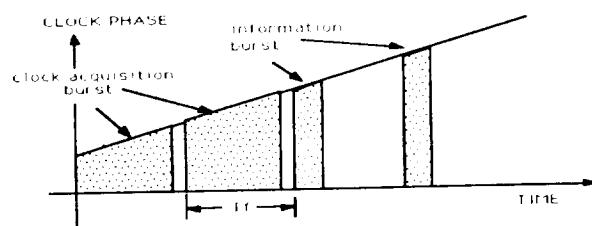


SYMBOL CLOCK ACQUISITION

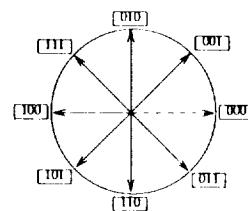


$$\text{phase slope} = (B_1 - B_0)/T_f$$

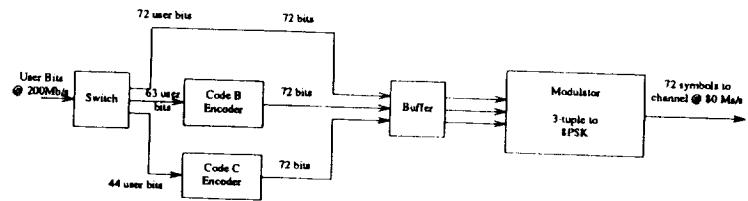
$$\text{phase correction} = \text{phase slope} \cdot (T_f - T_B) = (B_1 - B_0) \cdot (T_f - T_B)/T_f$$



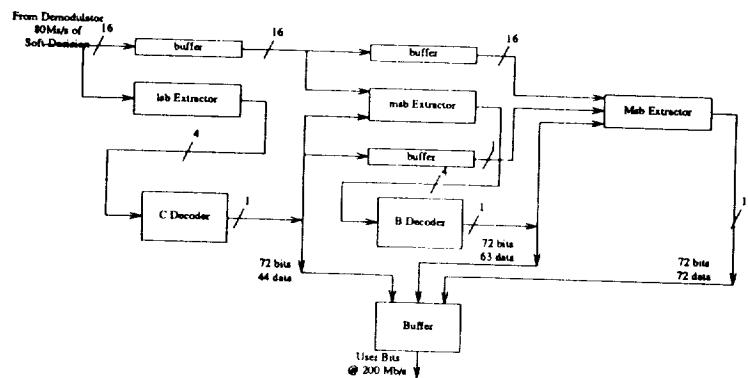
SIGNIFICANT BIT 8PSK TO 3-TUPLE MAPPING



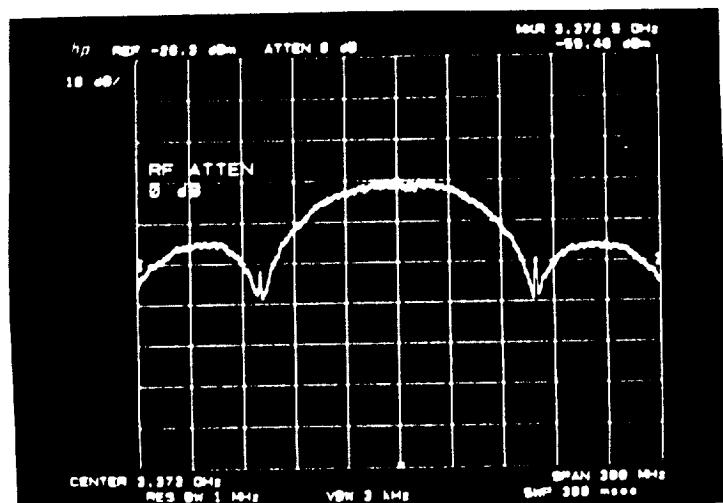
ENCODER SYSTEM



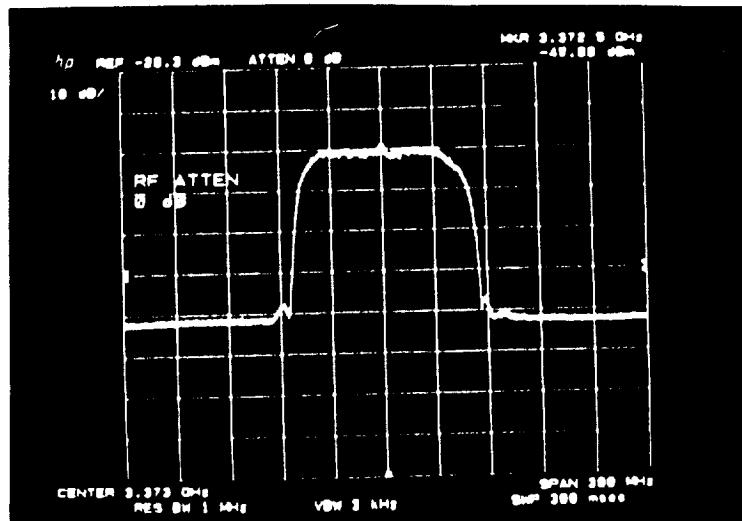
DECODER SYSTEM



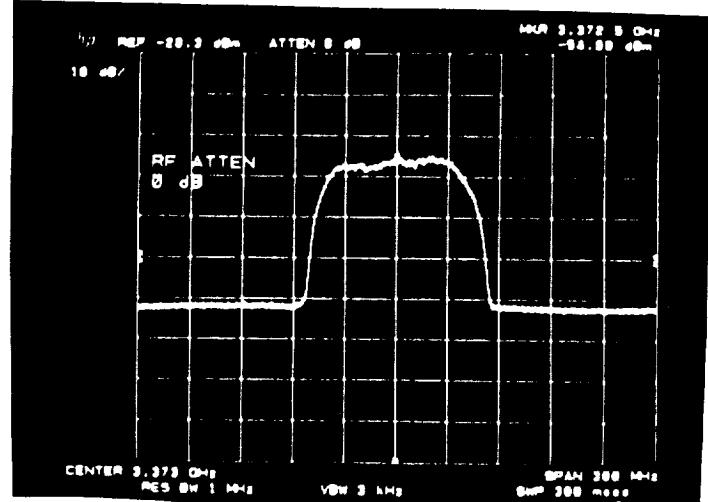
MODULATOR OUTPUT SPECTRUM



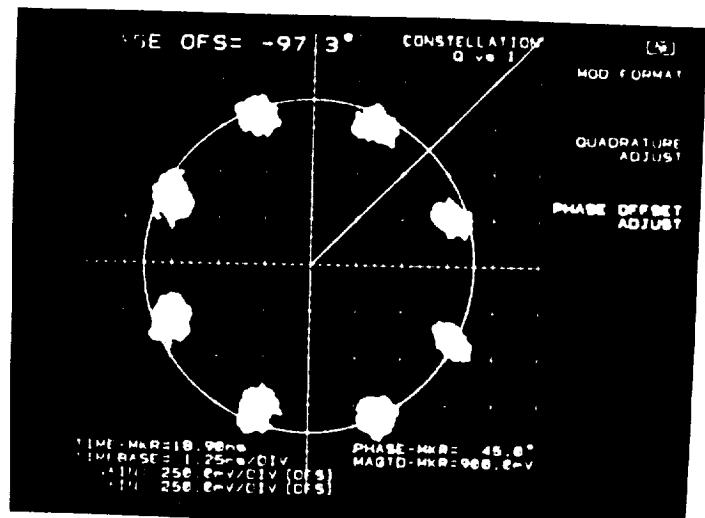
TRANSMITTER FILTER OUTPUT SPECTRUM



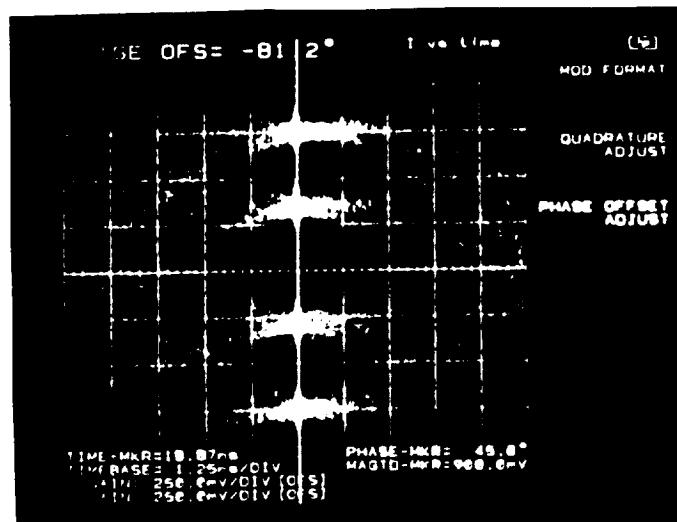
RECEIVER FILTER OUTPUT SPECTRUM



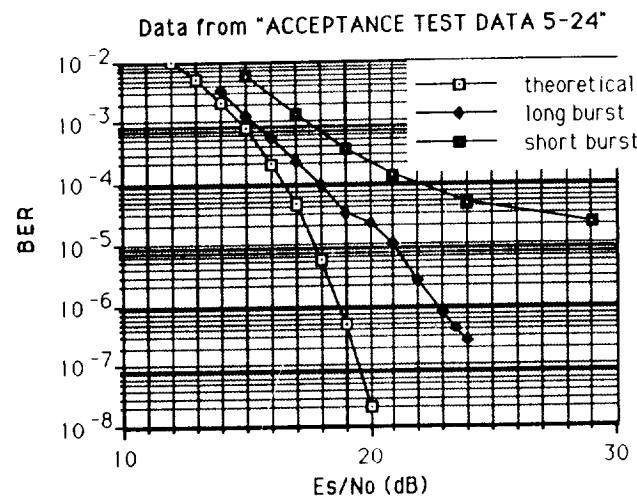
CONSTELLATION OUTPUT AT RECEIVER QUADRATURE DETECTOR



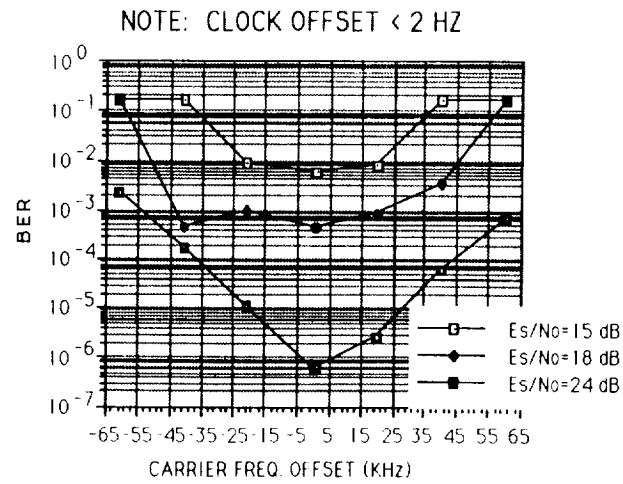
EYE PATTERN AT "I" SIDE OF QUADRATURE DETECTOR



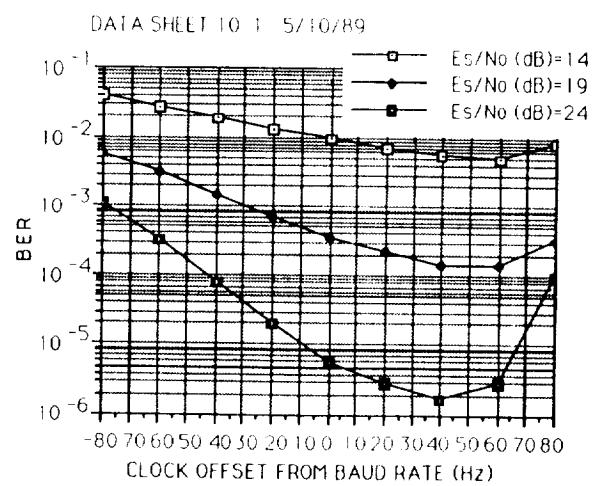
BIT ERROR RATE VERSUS Es/No IN AWGN FOR LONG AND SHORT BURSTS



BER VERSUS CARRIER FREQUENCY OFFSET

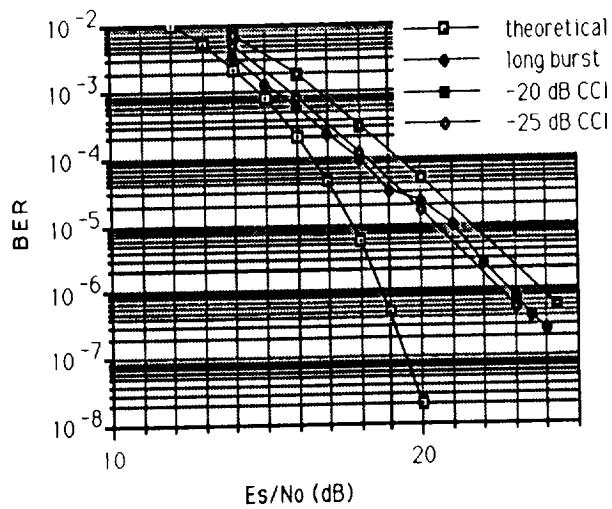


BER VERSUS CLOCK OFFSET FREQUENCY



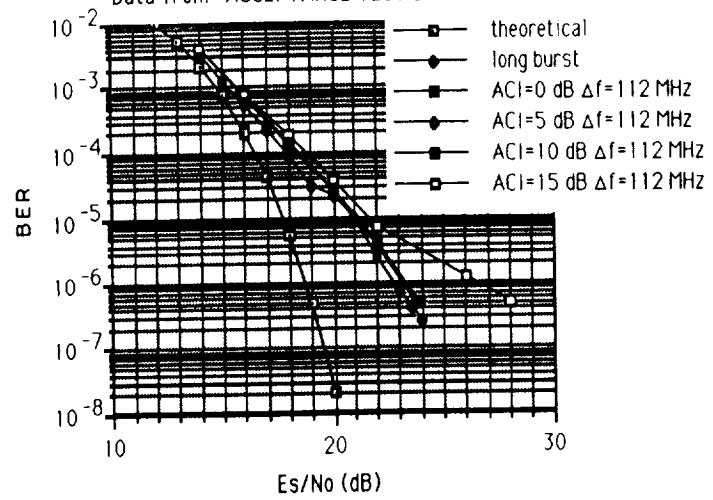
BER VERSUS ES/NO IN CCI

Data from "ACCEPTANCE TEST DATA 5-24"



BER VERSUS Es/No IN ACI FOR 112 MHz SPACING

Data from "ACCEPTANCE TEST DATA 5-24"



INPUT SPECTRUM TO RECEIVER WITH +20 dB ACI AT ± 112 MHz

